Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently Amended) A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

an oscillator having a tuning input, and an output with a tunable frequency responsive to the tuning input;

a mixer to mix the oscillator output with a second signal to produce a mixed signal; and

a phase detector outputting an error signal which is a function of a phase difference between the mixed signal and an input signal, the error signal being applied to the tuning input,

wherein the oscillator comprises a voltage controlled oscillator, the tuning input being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising a bandpass filter to filter the mixed signal before being applied to the phase detector, the filtered mixed signal comprising a difference frequency between the tuned frequency of the oscillator output and a frequency of the second signal, a limiter to limit the filtered mixed signal from the filter before being applied to the phase detector, a charge pump disposed between the phase detector and the oscillator, and a loop filter disposed between the charge pump and the oscillator.

Claims 2-14 (Cancelled).

15. (Currently Amended) A complimentary metal oxide semiconductor (CMOS) phase lock loop, comprising:

oscillator means for generating a first signal having a tunable frequency, the oscillating means comprising tuning means for tuning the frequency of the first signal;

mixer means for mixing the first signal with a second signal to produce a mixed signal; and

detector means for detecting a phase difference between the mixed signal and an input signal, and generating an error signal which is a function of the phase difference, the tuning means being responsive to the error signal,

wherein the oscillator means comprises a voltage controlled oscillator, the tuning means being responsive to a voltage of the error signal, the CMOS phase lock loop further comprising filter means for filtering the mixed signal before being applied to the detector means, the filtered mixed signal comprising a difference frequency between the tuned frequency of the first signal and a frequency of the second signal, means for limiting the filtered mixed signal from the filter means before being applied to the detector means, current means for sourcing current to the tuning means responsive to the error signal, and means for filtering the current sourced error signal from the current means before being applied to the tuning means.

Claims 16-28 (Cancelled).

29. (New) The CMOS phase lock loop according to claim 1, wherein the CMOS phase lock loop is integrated onto a single integrated circuit (IC) chip.

30. (New) The CMOS phase lock loop according to claim 15, wherein the CMOS phase lock loop is integrated onto a single integrated circuit (IC) chip.

31. (New) The CMOS phase lock loop according to claim 1, wherein the input signal comprises a transmitter intermediate frequency (IF) input signal.

32. (New) The CMOS phase lock loop according to claim 15, wherein the input signal comprises a transmitter intermediate frequency (IF) input signal.

33. (New) The CMOS phase lock loop according to claim 1, wherein the oscillator is an off-chip oscillator.

34. (New) The CMOS phase lock loop according to claim 15, wherein the oscillator means is an off-chip oscillator means.

35. (New) The CMOS phase lock loop according to claim 1, wherein the mixer operates at a lower clock frequency than the voltage controlled oscillator.

36. (New) The CMOS phase lock loop according to claim 15, wherein the mixer means operates at a lower clock frequency than the voltage controlled oscillator.

37. (New) The CMOS phase lock loop according to claim 1, wherein the CMOS phase lock loop is used with a transmitter in a wireless communication device.

38. (New) The CMOS phase lock loop according to claim 15, wherein the CMOS phase lock loop is used with a transmitter in a wireless communication device.

39. (New) The CMOS phase lock loop according to claim 1, wherein the CMOS phase lock loop is part of a wireless communication device.

40. (New) The CMOS phase lock loop according to claim 15, wherein the CMOS phase lock loop is part of a wireless communication device.

41. (New) The CMOS phase lock loop according to claim 39, wherein the wireless communication device supports communications using orthogonal frequency division multiplexing.

42. (New) The CMOS phase lock loop according to claim 40, wherein the wireless communication device supports communications using orthogonal frequency division multiplexing.

43. (New) The CMOS phase lock loop according to claim 39, wherein the wireless communication device supports communications using spread spectrum modulation.

44. (New) The CMOS phase lock loop according to claim 40, wherein the wireless communication device supports communications using spread spectrum modulation.

45. (New) The CMOS phase lock loop according to claim 39, wherein the wireless communication device supports communications using frequency hopping.

46. (New) The CMOS phase lock loop according to claim 40, wherein the wireless communication device supports communications using frequency hopping.

47. (New) The CMOS phase lock loop according to claim 39, wherein the wireless communication device supports communications using direct sequence spread spectrum modulation.

48. (New) The CMOS phase lock loop according to claim 40, wherein the wireless communication device supports communications using direct sequence spread spectrum modulation.